RoHS COMPLIANT

MICRO DISPLAY FOR NED APPS.

P/N: DSQ-5933-S000

LCoS Display Module for HMD/HUD/Pico Projector/AV Projector

FEATURES

- Single panel Liquid Crystal on Silicon (LCoS) with Display Controller
- 0.5" active display diagonal
- High definition (720P, 1280x720) array of 8.6 μm mirrors
- High refresh rate (up to 400Hz) for Field Sequential Color
- Gamma corrected 8-bit gray depth
- Low power consumption
- Embedded LED driver
- Embedded DC-DC converter
- High speed LVDS interface: 4 channel x 800 Mbps
- High reflectivity over 82%
- Contrast ratio 500:1 (at FSC driving)
- Active area 11.008 mm x 6.192 mm
- Module size 25.0 mm x 11.0 mm x 4.05 mm
- Power consumption 150 mW
- Fast VA (Vertical Alignment) LC mode
- High voltage LCoS process
- RoHS compatible package

FUNCTIONAL BLOCK DIAGRAM

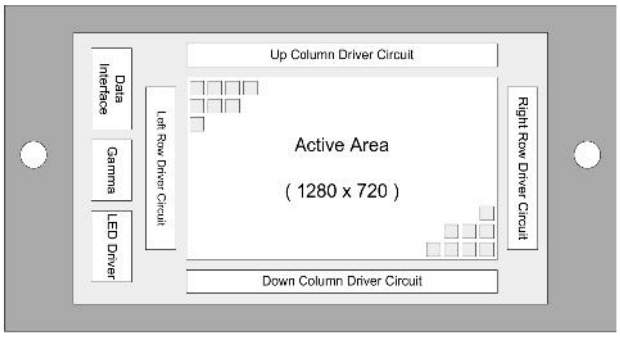

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The RDP501H is a highly integrated LCoS display module for single panel optical display system such as HMD (Head Mounted Display), HUD (Head-Up Display) and Pico Projector. It operates over 400 Hz refresh rate. It includes RGB LED driver, low voltage differential signal receiver and power-down detection circuit. The fast speed differential signal receiver, which receives LVDS format, interfaces fast speed parallel digital signals (4channel x 8bit) and controls signals for high frame rate of panel. The LVDS interface makes RDP501H be able to long path connection and high frame rate display, which enables panel to apply to single panel system such as HMD, HUD and Pico Projector.

For enhanced gray scaling performance, gamma corrected Resistor string and gamma tab voltages are fully programmable. The RGB LED driver supports RGB LEDs as light source of applications.

APPLICATIONS

- **Head Mounted Display**
- **Head Up Display**
- **Pico Projector**
- **AV Projector**

PRODUCTION HIGHLIGHTS

1. High frame rate for Field Sequential Color of single panel optical system
2. Differential Signal interface for long path
3. Embedded LED Driver
4. Low power consumption

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS

Table 1. DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Driver Power Supply Voltage	V_{DDH}	10.0	13.2	14.5	V
Logic Power Supply Voltage	V_{DDL}	1.7	1.8	2.0	V
LED Power Supply Voltage[1]	V_{LED}	2.0	5.0	12.0	V
DIGITAL INPUT/OUTPUT PINS					
Maximum Low Input Voltage	V_{IL}		1.25 - 0.125		V
Minimum High Input Voltage	V_{IH}		1.25 + 0.125		V
Maximum Low Output Voltage	V_{OL}			0.9x V_{DDL}	V
Minimum High Output Voltage	V_{OH}	VSS+ 0.5			V
High Level Input Current (V_{IN} = VDDIO)	I_{IH}			10	µA
Low Level Input Current (V_{IN} = GND)	I_{IL}	−10		10	µA
POWER CONSUMPTION[2]					
Total Power Consumption	P		TBD		mW
13.2V sub Total Power consumption					mW
Op-amp: (Vdata = ±6.75V)					mW
(Vdata = ±3V)					mW
Others:					mW
1.8V sub Total Power consumption					mW
LVDS / Others (800Mbps→420Hz)					mW
LED Power Consumption(V_{LED})			TBD		mW

NOTES

[1] In case of RDP501H internal LED driver used. It depends on LED specification.

[2] TA = 25°C, VDDH = 13.2V, VDDL = 1.8V, VDDLED = 5.0V supplies, unless otherwise noted.

ELECTRO-OPTICAL CHARACTERISTICS

T_A = 25°C, all VDDH = 13.2V, VDDL = 1.8 V supplies, unless otherwise noted.

Table 2. Optical Characteristics

Parameter		Conditions	Symbol	Min	Typ	Max	Unit
Contrast ratio		FSC operating	CR	-	TBD	-	
Reflectivity		λ = 550 nm			TBD		%
Response time	ON Time	10%--> 90%	T_{ON}		TBD		msec
	OFF Time	90%-->10%	T_{OFF}		TBD		
V-T(R) Characteristics	V90	λ = 550 nm	VT90		TBD		V
	V50		VT50		TBD		
	V10		VT10		TBD		
Flicker					TBD		
Crosstalk					TBD		

OPTICAL-MECHANICAL SPECIFICATIONS

Table 3. Optical/Mechanical Specifications

Parameter	Min	Typ.	Max	Unit
Display Resolution of active are		1280 x 720		
Active (Display) area size		11.008 x 6.192		mm
Pixel pitch		8.6 x 8.6		µm
Fill factor		91.1		%
Module dimension		25.0 (W)x 11.0 (H) x 4.05 (T)		mm

POWER SEQUENCE SPECIFICATIONS

Timing sequence requirements must be met during power-on and power-off of the display panel. The required control sequence of the display panel is shown in the following Power-on and Power-off Control Sequence figure, and the timing requirements are shown in the Sequence specification table.

Table4.Power on sequence specification

Parameter	Symbol[1]	Min	Unit
Power-Up Setup Margin 1.2V 1.8V, 3.3V		Don't care	
RESETB	R	1	ms
RESETB(Toggling)[1]	T	1	ms
Internal Booting Timing	Booting	500	ms
DISP_BTN(Internal Toggling)[2]	T'	1	ms
Reset time(Internal Control)	Reset Time	1000	ms
DCDC_PD (Internal Control)	A	50	ms
Main Supply for Panel (VDDH)	B	10	ms
LED Supply	C	10	ms
DCDC_PD Disable (After Reset, internal Control)	A'	50	ms
Main Supply (VDDH)	B'	10	ms
LED Supply	C'	10	ms
I2C Access(Internal access by MICOM)[3]	Access Time	1000	ms

NOTES
[1]RESETB(Pin#A3) Toggling
[2]Internal MICOM used only. Do not access this pin during this time.
[3]Do not access from external MCU during this time for safety.

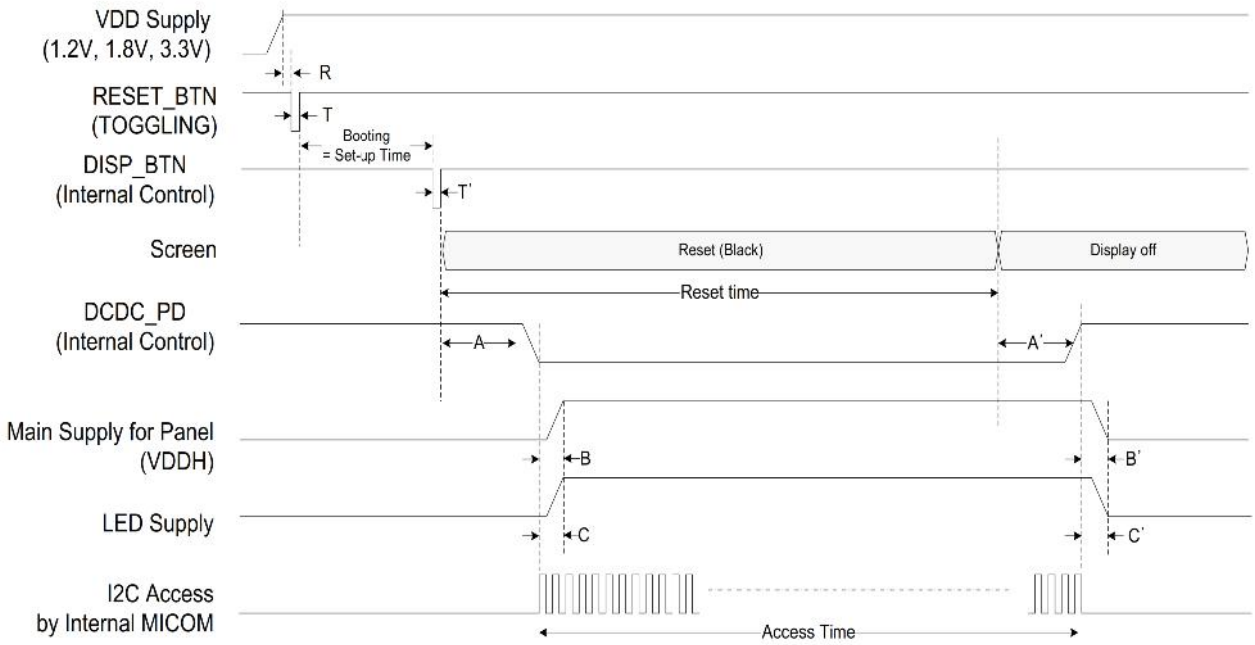

Figure 2. Power On & Digital Timing Diagram

Table5.Power off sequence specification

Parameter	Symbol[1]	Min	Unit
DISP_BTN(Toggling)[1]	T	1	ms
DCDC_PD(Internal Control)	A	50	ms
Main Supply for Panel (VDDH)	B	10	ms
LED Supply	C	10	ms
VDD Supply(1.2V, 1.8V, 3.3V)	D	10	ms

NOTES
[1] To Power Off reset, DISP_BTN(Pin#C12) toggling.

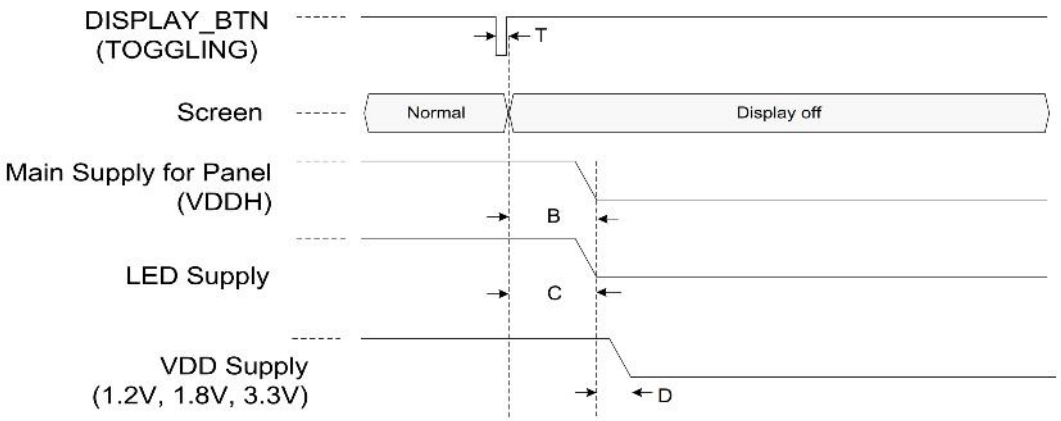

Figure 3. Power Off & Digital Timing Diagram

Table6. Display on sequence specification

Parameter	Symbol[1]	Min	Unit
DISP_BTN (Toggling)[1]	T	1	ms
Display on	Display on	150	ms
DCDC_PD(Internal Control)	A	50	ms
Main Supply for Panel (VDDH)	B	10	ms
LED Voltage Supply	C	10	ms

NOTES
[1] Display on signal (DISP_BTN(Pin#C12) toggling)

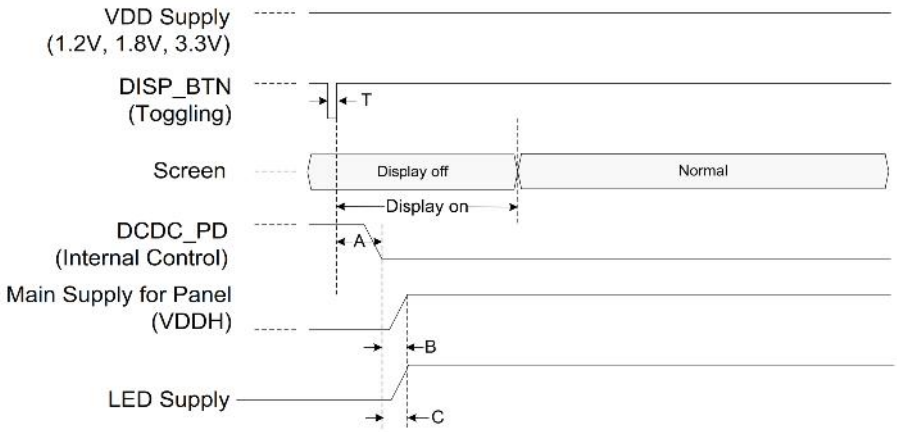

Figure 4. Display on & Digital Timing Diagram

Table7. Display off sequence specification

Parameter	Symbol[1]	Min	Unit
DISP_BTN (Toggling)[1]	T	1	ms
Display off	Display off	150	ms
DCDC_PD(Internal Control)	A	50	ms
Main Supply for Panel (VDDH)	B	10	ms
LED Supply	C	10	ms

NOTES
[1] Display off signal (DISP_BTN(Pin#C12) toggling)

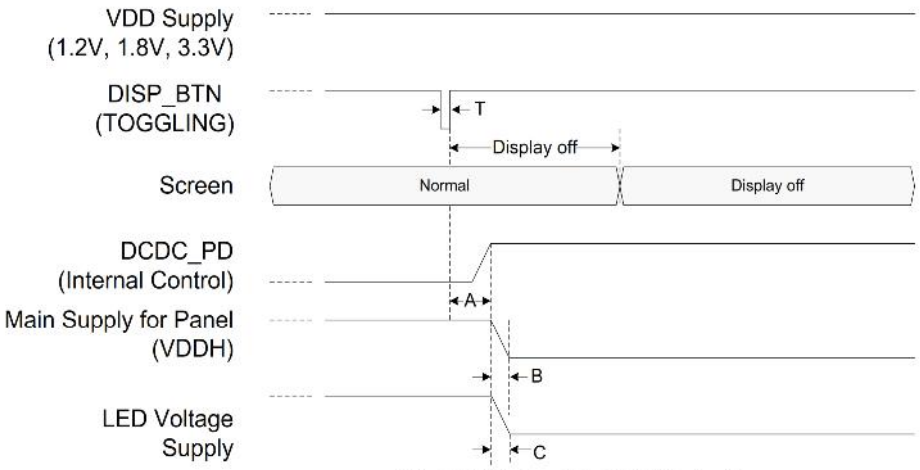

Figure 5. Display off & Digital Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table8. Absolute Maximum Ratings

Parameter	Rating
VDDH (VDD13.2V)	-0.3V to +16 V
Core Supply (VDD1.8V)	-0.3V to +3.6V
Operating Temperature Range	0°C to +50°C
Storage Temperature Range	–20°C to +80°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

FPC-PIN DESCRIPTION

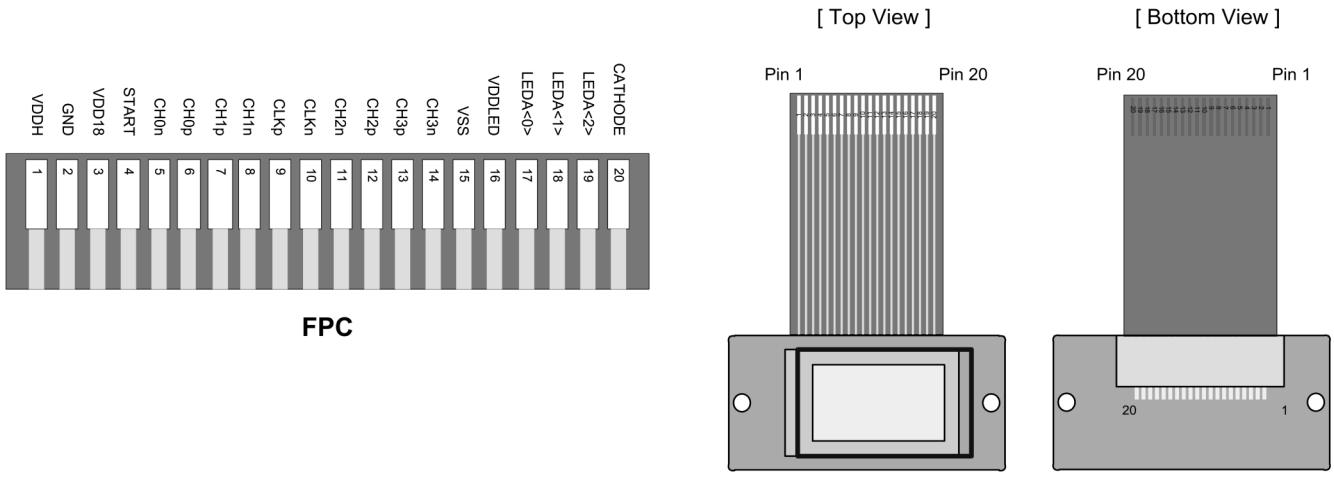

Figure 6. FPC Pin Configuration (TOP VIEW)

Table9. Pin Function Descriptions (Default Mode)

Pin No.	Mnemonic	I/O Type[1]	Description
1	VDDH	P	Analog Power Supply
2	VSS	GND	Analog/Digital Ground
3	VDD18	P	Digital Power Supply
4	START	DI	Command & Option Packet Strobe
5	CH0n	DI	Serial Data Input. inverting LVDS Differential Input
6	CH0p	DI	Serial Data Input. Non-Inverting LVDS Differential Input
7	CH1p	DI	Serial Data Input. Non-inverting LVDS Differential Input
8	CH1n	DI	Serial Data Input. Inverting LVDS Differential Input
9	CLKp	DI	Non-inverting LVDS differential Clock Input
10	CLKn	DI	Inverting LVDS Differential Clock Input
11	CH2n	DI	Serial Data Input. inverting LVDS Differential Input
12	CH2p	DI	Serial Data Input. Non-Inverting LVDS Differential Input
13	CH3p	DI	Serial Data Input. Non-inverting LVDS Differential Input
14	CH3n	DI	Serial Data Input. Inverting LVDS Differential Input
15	VSS	GND	Analog/Digital Ground
16	VDDLED	P	LED Power Supply
17	LEDA<0>	AO	RED LED Anode
18	LEDA<1>	AO	GREEN LED Anode
19	LEDA<2>	AO	BLUE LED Anode
20	CATHODE	AI	LED Common Cathode

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DB = digital bidirectional, P = power, GND = Ground.

THEORY OF OPERATION

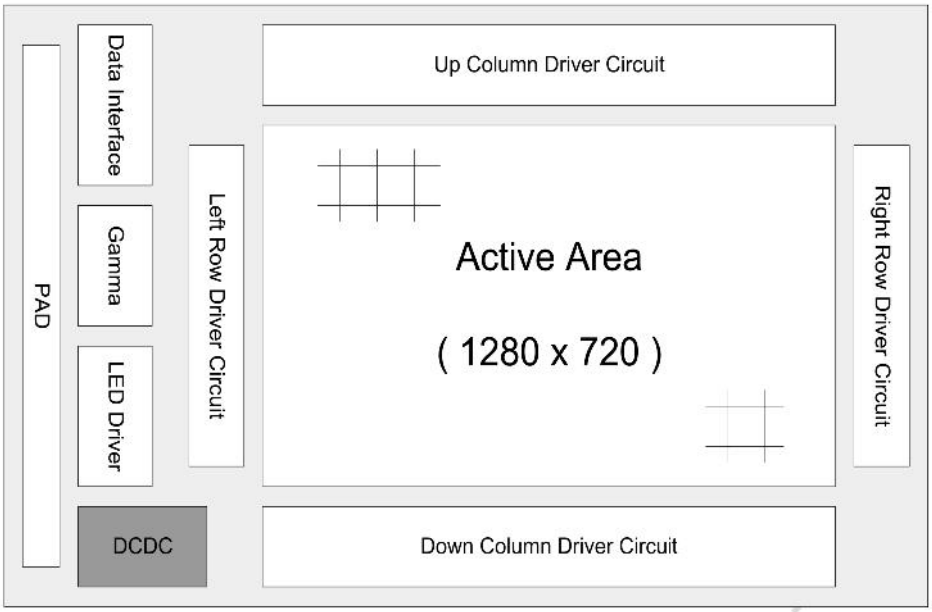

Figure 7. *Block diagram*

MIRROR ARRAY (ACTIVE AREA)

The real size of Active area is 11.008mm x 6.192mm. It includes 1280 x 720 pixels for each 8.6um square. Each Pixel's voltage is referenced to a common electrode voltage. The Contrast Ratio is 500:1 at FSC driving mode and Reflectivity shows over 82%.

UP/DOWN COLUMN DRIVER CIRCUIT

Column driver circuits are consists of Shift register and Latch array with clock buffer, DAC and Op-amp array. The function of these circuits drives signal voltage to each column pixel.

LEFT/RIGHT ROW DRIVER CIRCUIT

Column driver circuits are consists of shift register and level shifter. The function of these circuits drives selection signal voltage to each row pixel.

DATA INTERFACE

To interface with high speed, it includes LVDS receiver with 4 data channels. The speed of clock channel is 400MHz Max.

GAMMA R-STRING & BUFFER

The 8-bits Gamma Weighted resistor string buffer outputs 0.2 ~ 11.8V. It supports 10MHz frequency Min.

LED DRIVER

The LED Driver incorporates 8-bit D/A converters to transfer input digital data into output analog voltage for each channel.

APPLICATIONS INFORMATION

TYPICAL APPLICATION

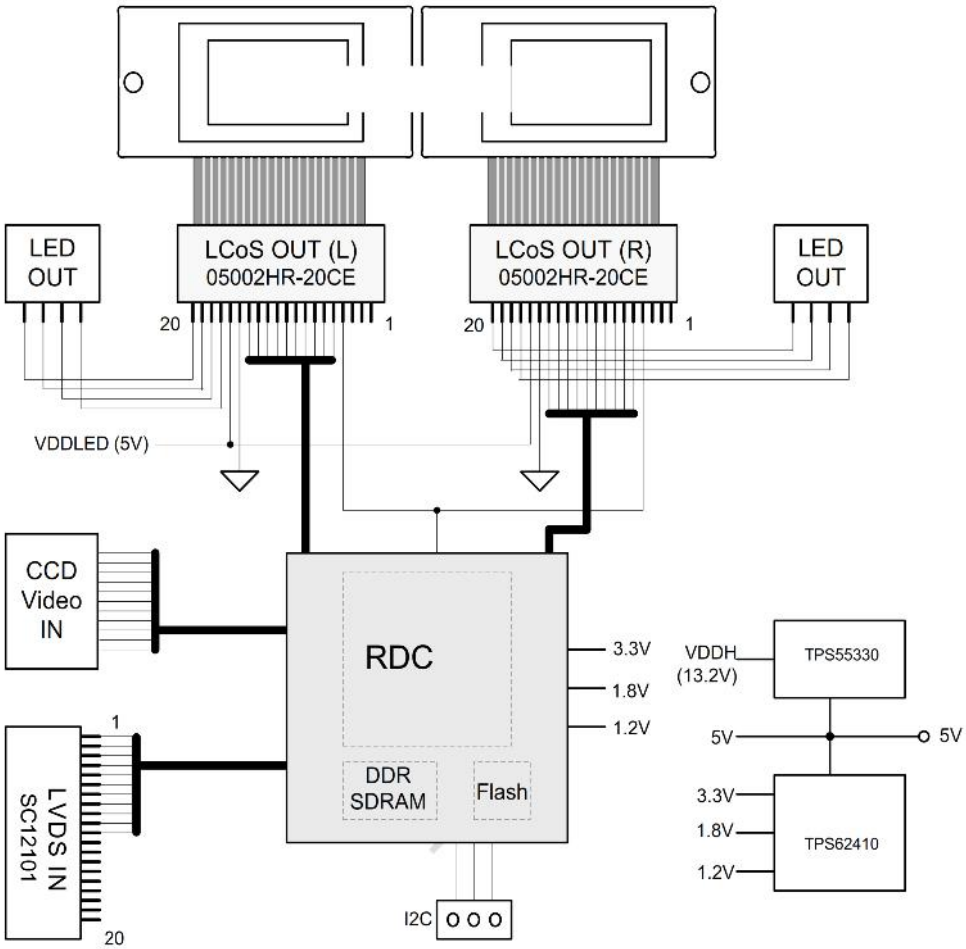

Figure 8. Typical Application

GAMMA R-STRING & TAB VOLTAGES

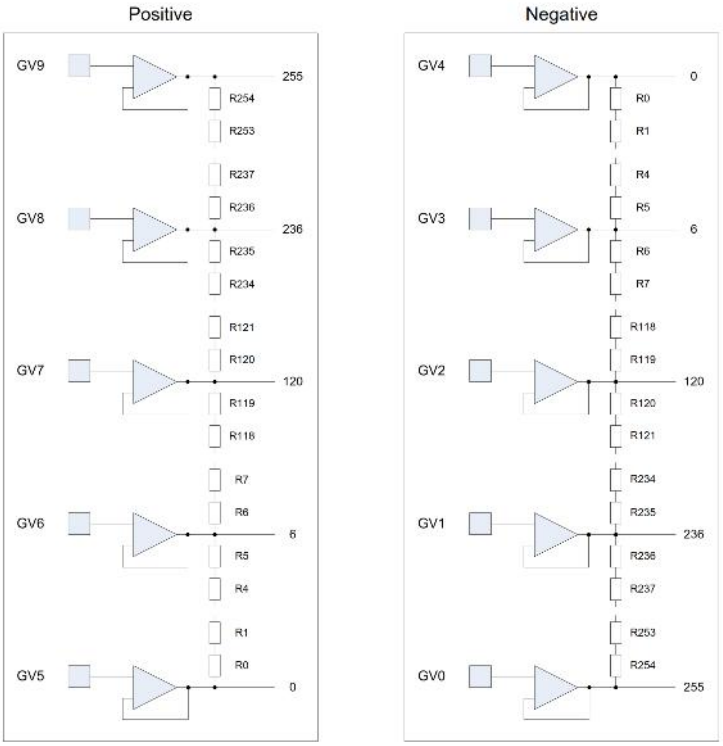

Figure 18. Relationship between external voltages and internal gamma-corrected R-string Circuits

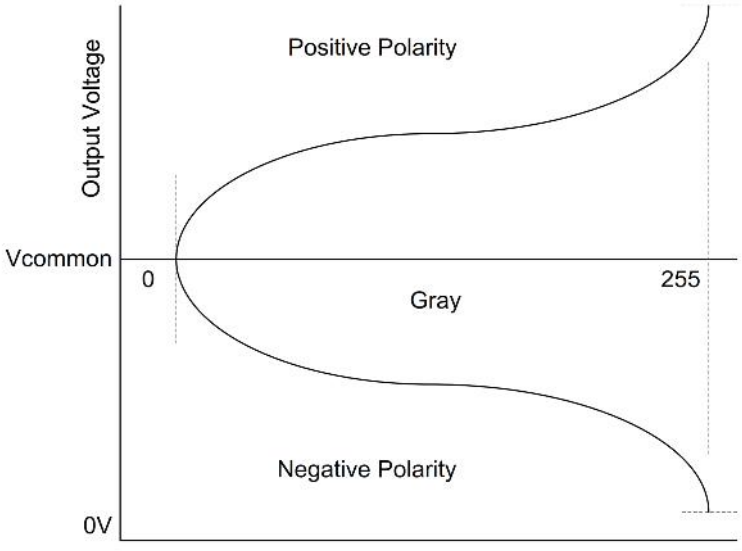

Figure 19. Gamma correction curves

LED OUTPUT

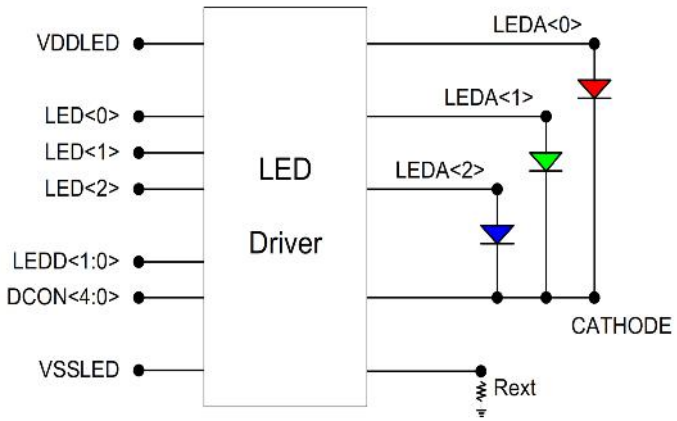

Figure 20. LED Driver

NOTES: VDDLED=5V, Rext = 100k on Panel Board

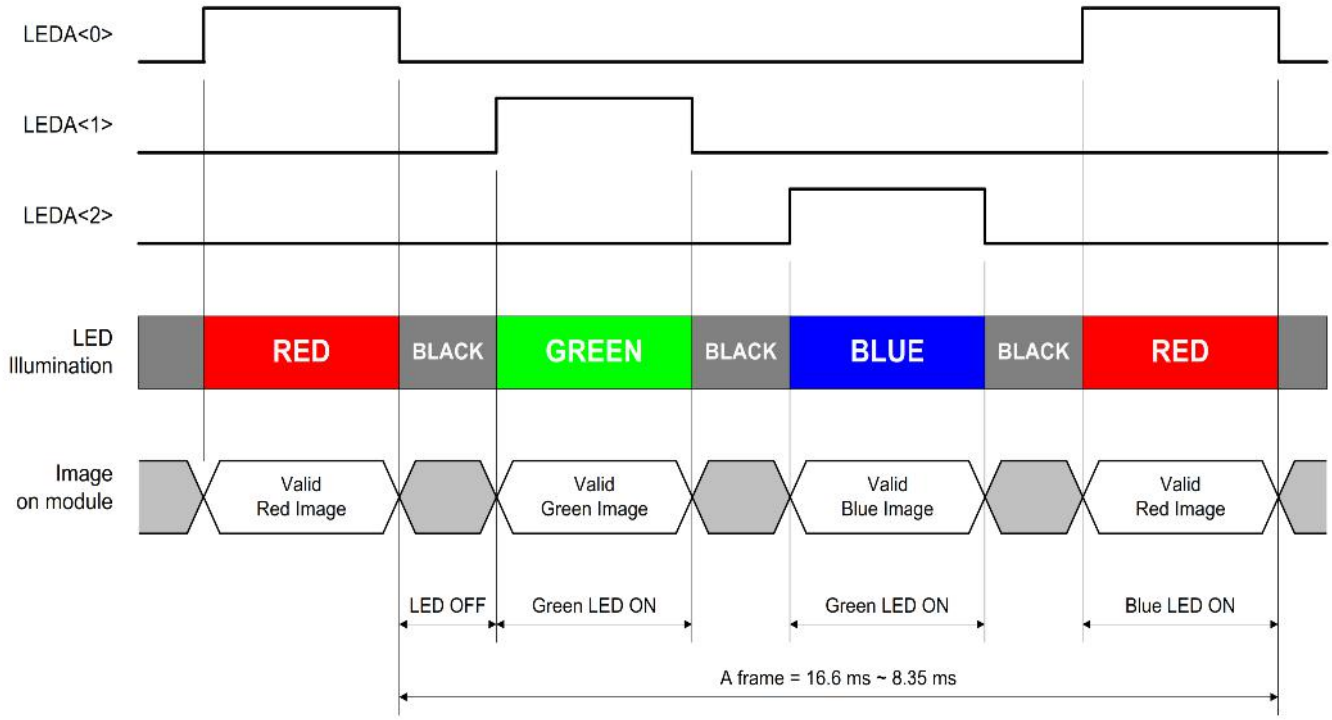

Figure 21. LED Timing Diagram

OUTLINE DIMENSIONS

FPC CONNECTOR TYPE

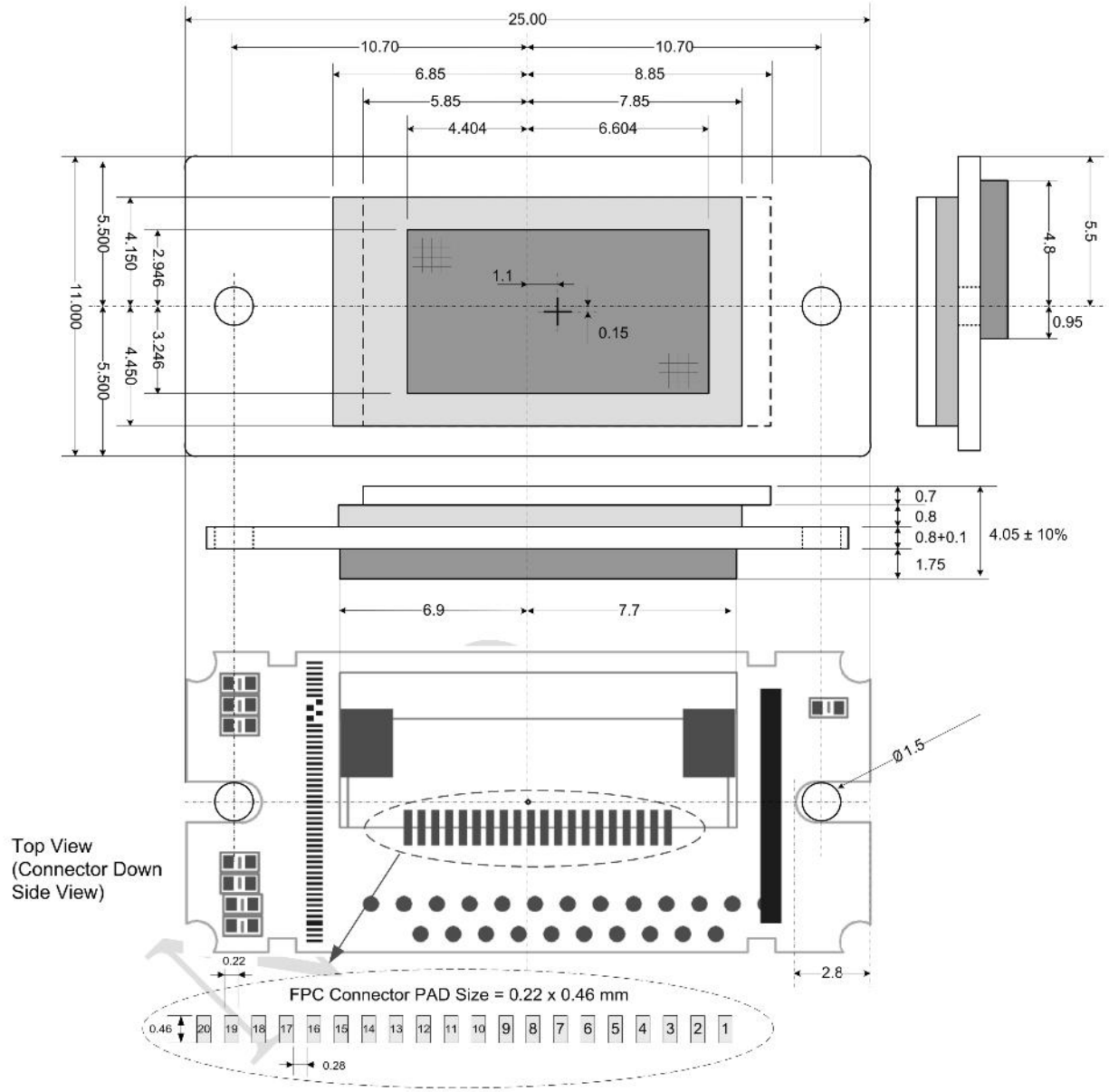

Figure 22. Module PCB
25 mm ×11 mm Body Dimensions shown in millimeters

FPCB connector : TF31-20S-0.5SH by HRS (The connector is changeable without notice.)