AMOLED 1.39” FOR WEARABLE APPS.

P/N: DFK-6133-S000

1.0 GENERAL DESCRIPTION

1.1 Introduction

This AMOLED display module features a high-resolution 454x454 pixel matrix with a four-wire SPI interface, supporting fast data transmission, making it suitable for a wide range of embedded systems and portable devices. The compact screen is driven by the SH8601A display controller, providing high-quality image display, ideal for applications requiring small display modules. The display offers wide viewing angles and high contrast, ensuring clear detail rendering, making it suitable for both industrial and consumer electronic products. Its well-designed interface enables easy connection to various main controllers, providing stable performance with low power consumption, making it an ideal choice for projects requiring both efficiency and low energy usage.

1.2 Features

- High Resolution Display: 1.39-inch AMOLED, 454x454 pixels.
- Multiple Interfaces: SPI and MIPI support.
- Capacitive Touch Screen: Responsive and accurate.
- Low Power Consumption: Ideal for battery-powered devices.
- Wide Temperature Range: -20°C to +70°C.
- High Luminance: 350 cd/㎡ typical.
- Rich Color Depth: 16.7 million colors.
- Compact Size: 42(H) x 42.6(V) x 2.227(D) mm.

1.3 General Specification

Item	Contents
Screen Size	1.39”
Display Mode	AMOLED
Resolution	454(H)*454(V)
Active Area	35.41(H)*35.41(V) mm
Module Size	42(H)42.6*(V)2.227*(D) mm
Color Arrangement	RGB Vertical Stripe
Interface	SPI/MIPI
Driver IC	SH8601A
Luminance(cd/㎡)	350(TYP)
View Direction	All View
Tough Mode	CTP
Tough IC	TMA525B
Color Depth	16.7M
Weight	

2.0 ELECTRICAL SPECIFICATIONS

2.1 DC Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Pin	Unit
Battery power Voltage	V_{BAT}		2.9	3.7	4.8		V
Digital Supply Voltage	V_{DDIO}		1.65	1.8	3.3		V
Logic high level input voltage	V_{IH_IO1}		$0.8V_{DDIO}$		V_{DDIO}	RESX	V
Logic low level input voltage	V_{IL_IO1}		0		$0.2V_{DDIO}$		V
Logic high level output voltage	V_{OH_IO1}	I_{OUT} = -1 mA	$0.8V_{DDIO}$		V_{DDIO}	TE	V
Logic low level output voltage	V_{OL_IO1}	I_{OUT} = +1 mA	0		$0.2V_{DDIO}$		V
Input high level leakage current	I_{IH}	$V_{IN} = V_{DDIO}$			1	RESX	uA
Input low level leakage current	I_{IL}	$V_{IN} = V_{ss}$	-1				uA
Operating current	$IVDDI_{OP}$	Frame freq.=60Hz, no load, SR_SET = 5'b10110, SPR function OFF			2.805		mA
	$IVCI_{OP}$				5.5		mA
Sleep current	$IVDDI_{LP}$	LP11 mode			850		uA
	$IVCI_{LP}$				50		uA
	$IVDDI_{ULPS}$	ULPS mode			833		uA
	$IVCI_{ULPS}$				50		uA
Deep steady current	$IVDDI_{DSLP}$				4		uA
	$IVCI_{DSLP}$				2		uA
ESD							kV

Note:The table above shows only the driver IC's power consumption.(MIPI I/F @0.5Gbps,white pattern)

V_{CI}=2.8V,V_{DDIO}=1.8V,TA=25℃

2.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Analog Supply Voltage	V_{CI}	-0.3	4.8	V
Digital Supply Voltage	V_{DDIO}	-0.3	4.0	V

3.0 Pin Definitions

3.1 Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

Pin Order	Symbol	Description
1	XRES	Device reset signal (0 : enable ; 1 : Disable)
2	VCI_EN	POWER IC Enable Input Voltage 1.8-3.3V
3	VPP	OTP——NC
4	GND	Ground
5	TE	Synchronous signal output from panel to avoid tearing effect
6	DSI_D0N	MIPI data negative signal
7	AM_SPI_CSX	SPI interface
8	DSI_D0P	MIPI data positive signal
9	AM_SPI_SCL	SPI interface
10	GND	Ground
11	AM_SPI_DCX	SPI interface
12	DSI_CLKN	MIPI strobe negative signal
13	AM_SPI_SDI	SPI interface
14	DSI_CLKP	MIPI strobe positive signal
15	AM_SPI_SDO	SPI interface
16	GND	Ground
17	ID(L)	Ground
18	VDDIO	Power supply for interface system
19	VBAT	AMOLED power

20	VDDIO	Power supply for interface system
21	VBAT	AMOLED power
22	VBAT	AMOLED power
23	VBAT	AMOLED power
24	VBAT	AMOLED power

3.2 CTP Input/Output Signal Interface

Pin Order	Symbol	Description
1	VCC(2V8)	Power supply for CTP: 2.8~3.3V
2	SCL(1V8)	CTP I2C clock input pin
3	SDA(1V8)	CTP I2C data input/output pin
4	EINT(1V8)	Interrupt request to the host
5	RST(1V8)	Reset pin for CTP
6	GND	System ground

4.0 Optical Characteristics

Test Condition: V_{DDIO}=1.8V,V_{CI}=2.8V,TA=25℃

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Remark
Luminance	-	θ=0°		300	350	-	cd/m²	Note1
Uniformity	-	Φ=0°		80	85	-	%	Note2
Viewing Angle	θL	Left	CR≥ 200	80	85	-	Deg.	Note3
	θR	Right		80	85	-		
	θT	TOP		80	85	-		
	θB	Bottom		80	85	-		
Constrast Ratio	CR	θ=0° Φ=0°		10000	100000	-	-	Note4
Response Time	Φ=0°			-	2	3	ms	Note5

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Remark
Color Coordinate of CIE 1931	X	Red	θ=0° Φ=0°	-	-	-	-	-
	Y			-	-	-		
	X	Green		-	-	-		
	Y			-	-	-		
	X	Blue		-	-	-		
	Y			-	-	-		
	X	White		0.29	0.32	0.35		
	Y			0.3	0.33	0.36		
NTSC Ratio	NTSC	CIE 1931		85	100	-	%	-
Flicker	-	-		-	-	-30	dB	-
Gamma	-	-		2.0	2.2	2.4	-	Note6
Crosstalk	ΔCT	-		-	-	3	-	Note7

Note 1: Luminance measurement

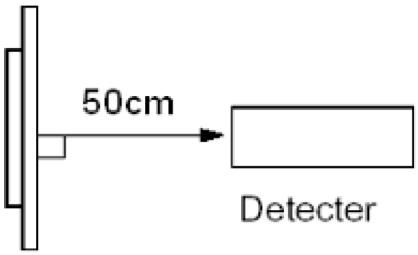
The test condition is measured on the surface of AMOLED module at 25℃

•Measurement equipment CS2000 or similar equipment (Field of view:1deg,Distance:50cm)

• Measuring surroundings: Dark room.

• Measuring temperature: Ta=25℃.

• Adjust operating voltage to get optimum contrast at the center of the display.



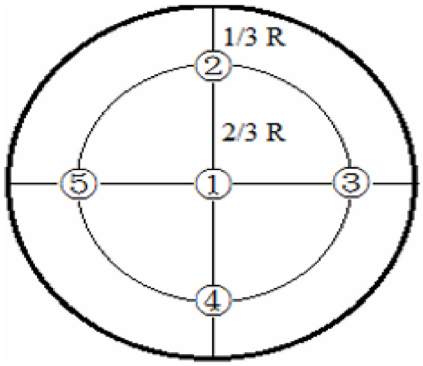
Note 2: Uniformity

•The luminance uniformity is calculated by using following formula:

△Bp = Bp (Min.) / Bp (Max.)×100 (%) Bp (Max.) = Maximum

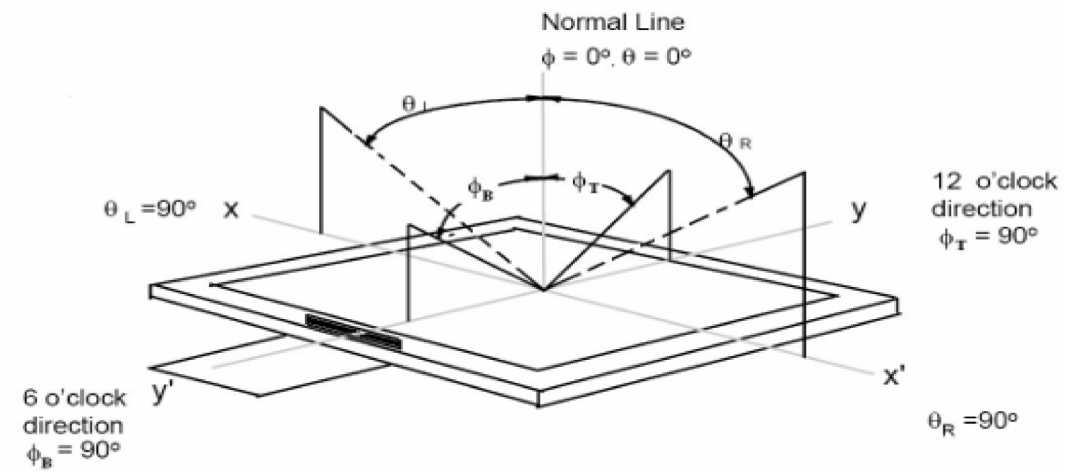
• brightness in 5 measured spots

• Bp (Min.) = Minimum brightness in 5 measured spots



Note 3: The definition of Viewing Angle

• Refer to the graph below marked by θ and Φ



Note 4: The definition of Contrast Ratio

• Refer to the graph below marked by θ and Φ

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When AMOLED is at “White” state}}{\text{Luminance When AMOLED is at “Black” state}}$$

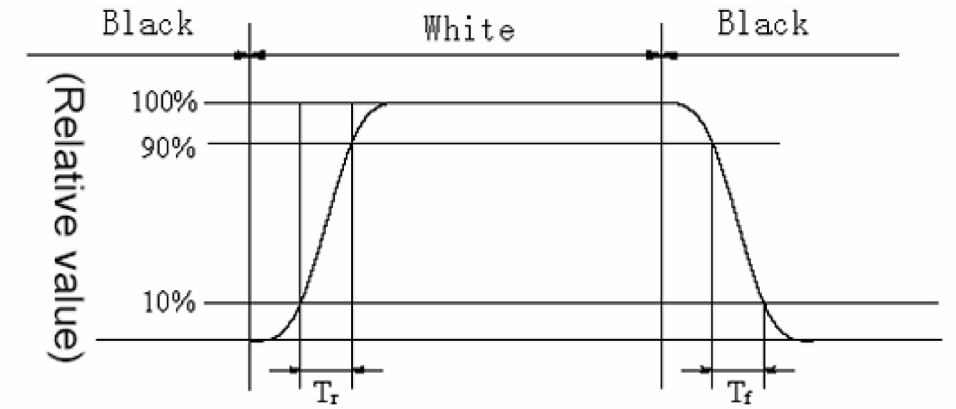
Note 5: Definition of Response time

• The output signals of a photo detector are measured when the input signals are changed from “black”

to "white" (Voltage falling time) and from "white" to "black" (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to the figure as below.

Note 6: Gamma curve

• The whole curve's tolerance must control within +/-0.3, test the gray scale below:



8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197,206, 214, 222, 230, 239, 255

Note 7: Crosstalk

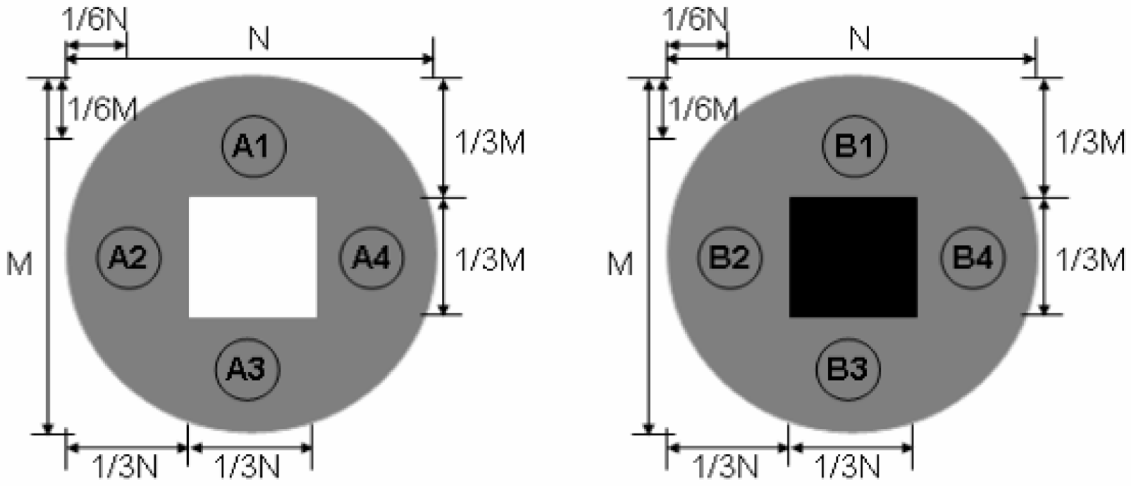
• There should be no visible cross-talk in the normal direction of the display when the two "Cross-talk Test Patterns" below are loaded.

△Bp (Max.) = Maximum value in △Bp1~△Bp4.

△Bp (Min.) = Minimum value in △Bp1~△Bp4.

△CT=△Bp (Max.)/ △Bp(Min.).

△CT must be less than 1.10



5.0 Reliability

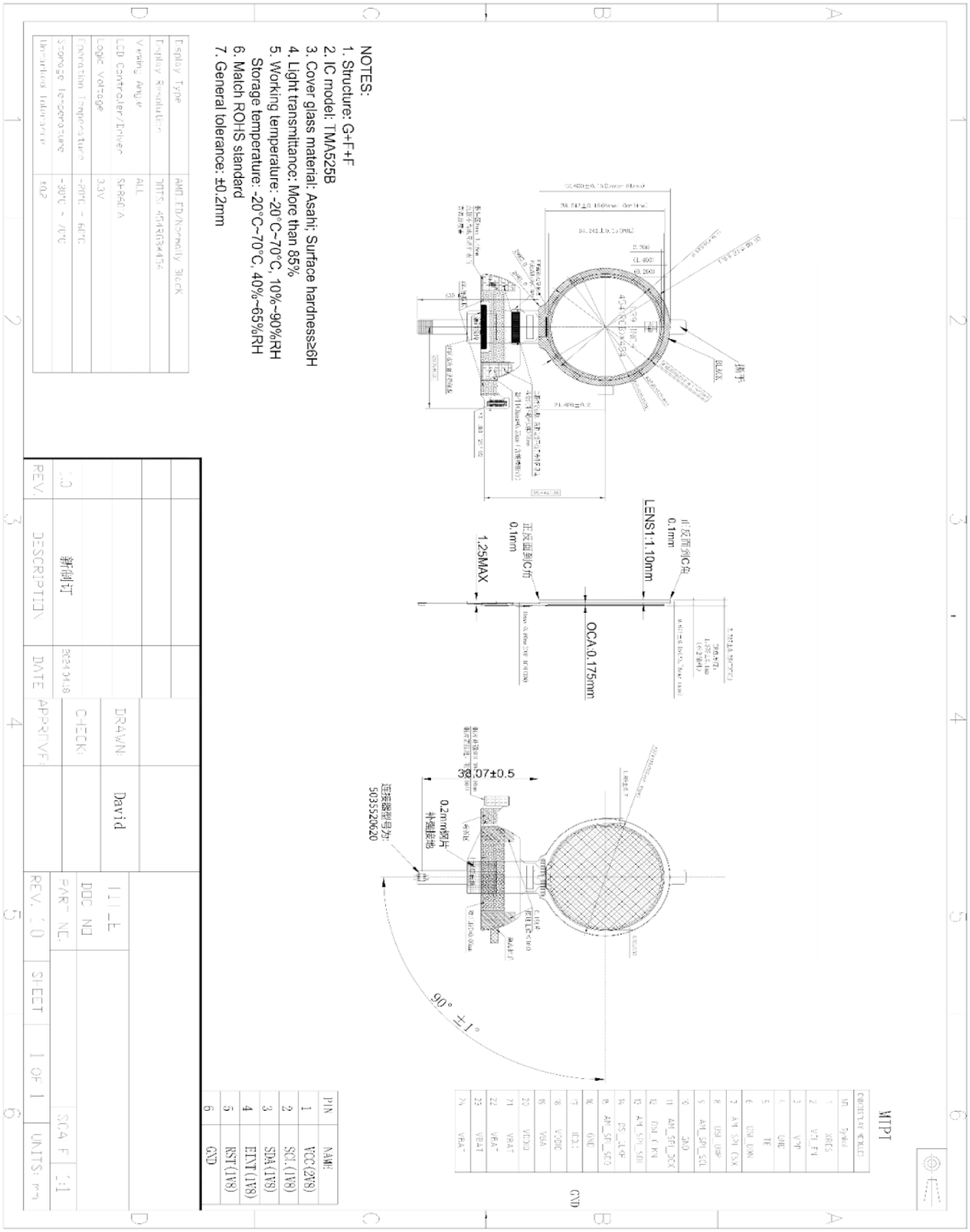
5.1 Environmental Requirements

Item	Conditions	Note
Operating Temperature	TA=-20°C ~ 60°C@72hrs	
Storage Temperature	TA=-30°C ~ 70°C@72hrs	
High Temp./Humi. Operation	TA=50℃,90%RH@72hrs	

5.2 Shock and Vibration

Test Item	Conditions
Thermal Shock	-30℃~70℃,Dwell for 30 min.30 cycles.

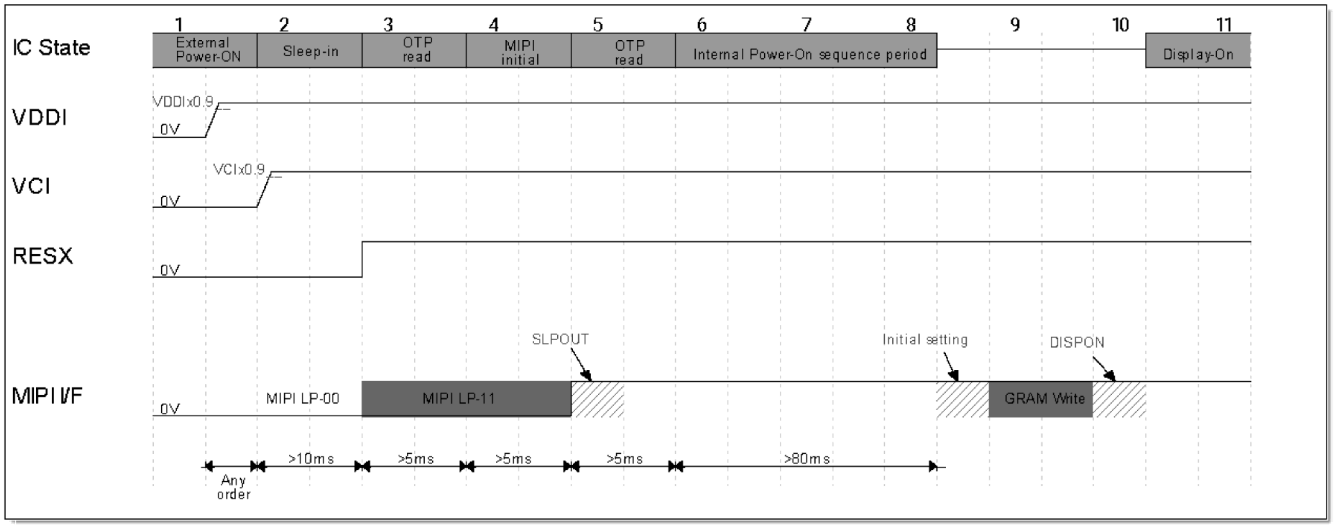
6.0 Mechanical Dimensions(mm)



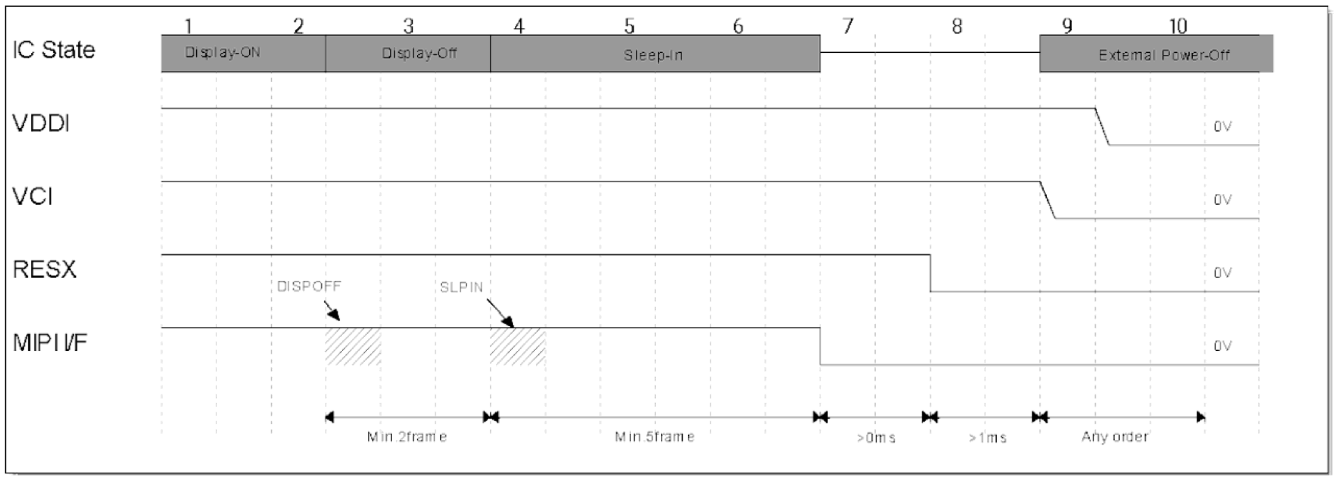
Item	Connctor MPN	Note
1	YXT-BB1F-24P-02	Main Connector
2	5035520620	TP Connector

7.0 Power Supply Sequence

7.1 Power on sequence



7.2 Power off sequence

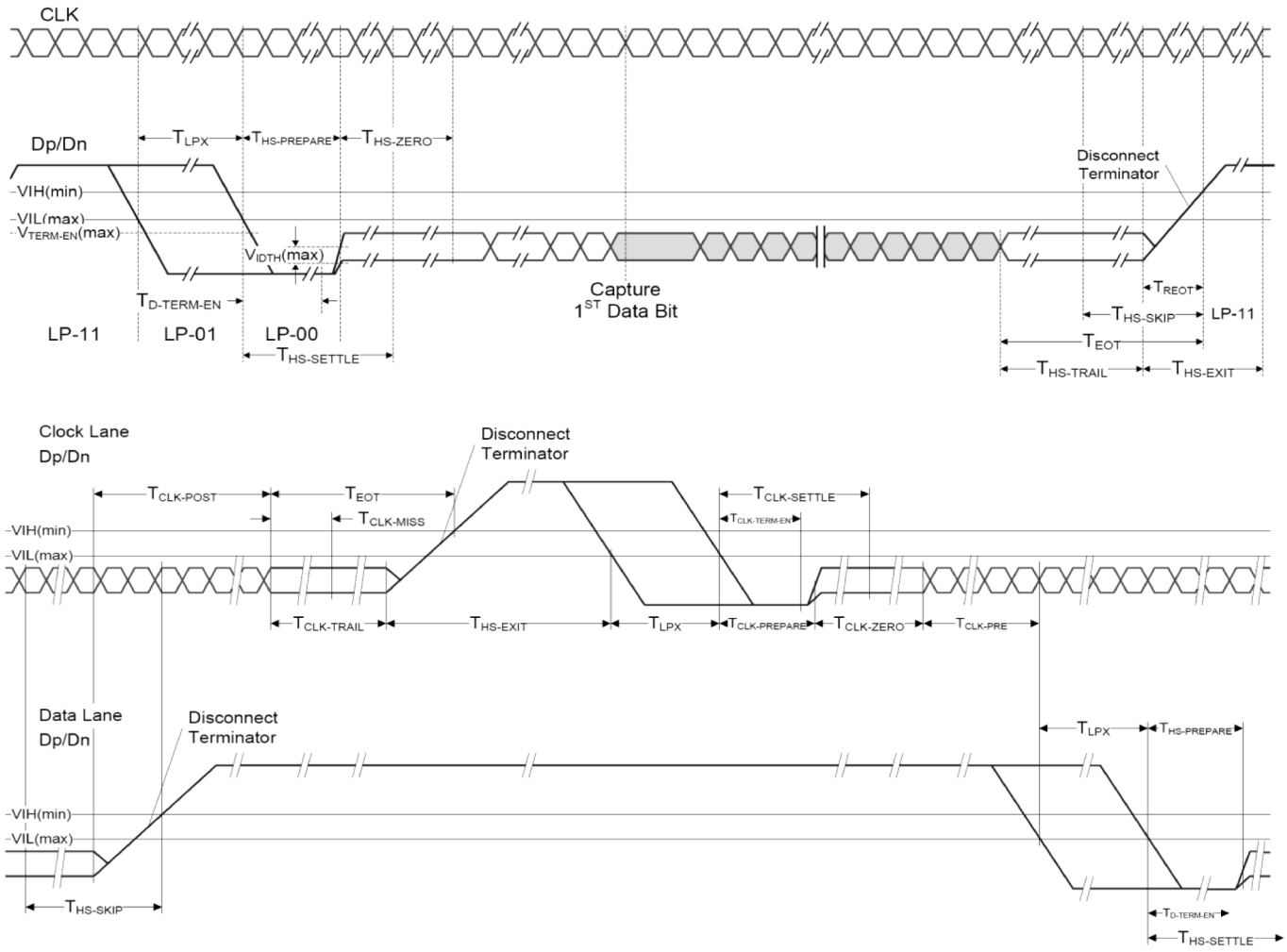


8.0 Description of Functions

8.1 AC Characteristics(MIPI)

8.1.1 High Speed Clock and Data transmission

Below Figure shows the sequence of the high speed data transmission.



The values in the following table require a clock tolerance no worse than 10% for implementation.

8.1.2 Global Operation Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-MISS}$	Time Out for receiver to detect absence ofClock transitions and disable the Clock Lane HS-R_X.	-	-	60	ns	1,6
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THSTRAIL to the beginning of	60ns+ 52 x UI	-	-		5

Symbol	Description	Min.	Typ.	Max.	Unit	Note
	$T_{CLK-TRAIL}$					
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	UI	
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns	6
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95	-	300		
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $T_{CLK-PREPARE}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns	5
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-		
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS.0 state prior to starting the Clock.	300	-	-		
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX}.	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4 x UI	-	6
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP.11 state following a HS burst.	-	-	105ns + n x 12 x UI	-	3,5
$T_{HS-EXIT}$	Time that the transmitter drives LP.11 following a HS burst.	100	-	-	ns	5
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP00 Line state immediately before the HS.0 Line state starting the HS transmission.	40 ns + 4 x UI	-	85ns + 6 x UI		
$T_{HS-PREPARE}$+ $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10 x UI	-	-		
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane	85ns + 6 x UI	-	145 ns + 10 x UI		6

RoHS COMPLIANT

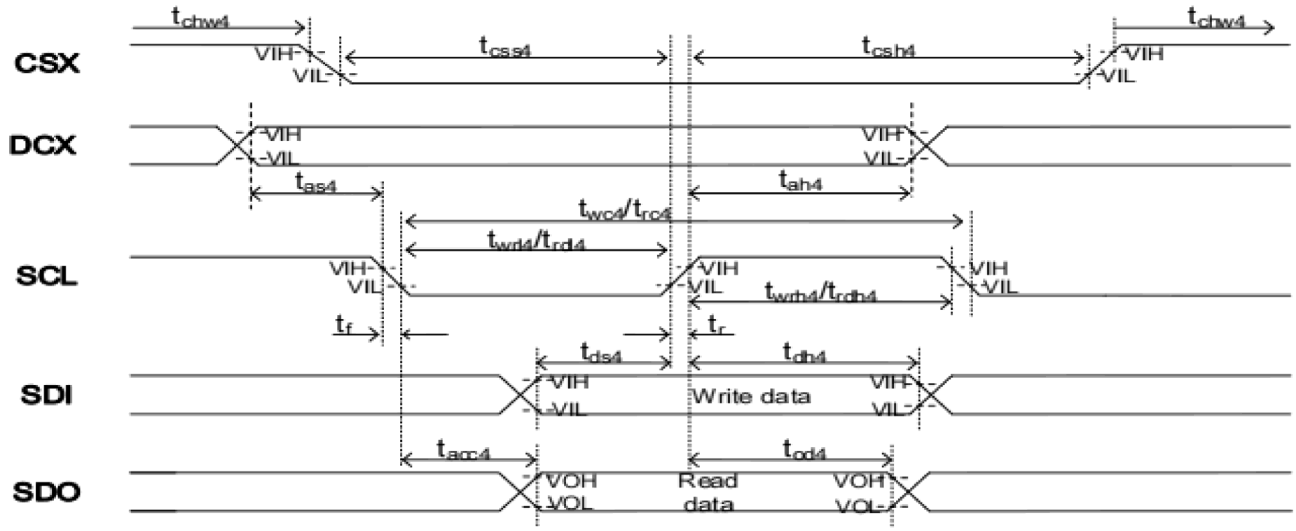
Symbol	Description	Min.	Typ.	Max.	Unit	Note
	HS transitions, starting from the beginning of $T_{HS-PREPARE}$.					
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	-	55ns + 4 x UI		
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	MAX (n x 8 x UI, 60ns + n x 4 x UI)	-	-		2, 3, 5
T_{LPX}	Transmitted length of any Low-Power state period	-	56.6	-		4,5
Ratio T_{LPX}	Ratio of T_{LPX}(MASTER)/ T_{LPX}(SLAVE) between Master and Slave side	2/3	-	3/2	-	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Tumaround.	5 x T_{LPX}			ns	5
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Tumaround.	4 x T_{LPX}				
$T_{TA-SURE}$	Time that the new transmitter waits after theLP.10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}	-	2 x T_{LPX}		
T_{WAKEUP}	Time that a transmitter drives a Mark-1state prior to a Stop state in order to initiate an exit from ULPS	1			ms	5

Note :

1. The minimum value depends on the bit rate,Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then Max.(a,b)=a,otherwise Max.(a,b)=b
3. Where n = 1 for Forward-direction HS mode and n=4 for Reverse-direction HS mode
4. T_{LPX} is an internal state machine timing reference.Externally measured values may differ slightly from the specified value due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

8.2 AC Characteristics(SPI 4 Wire)

8.2.1 MIPI DBI Type-C - Option3(SPI 4 Wire)

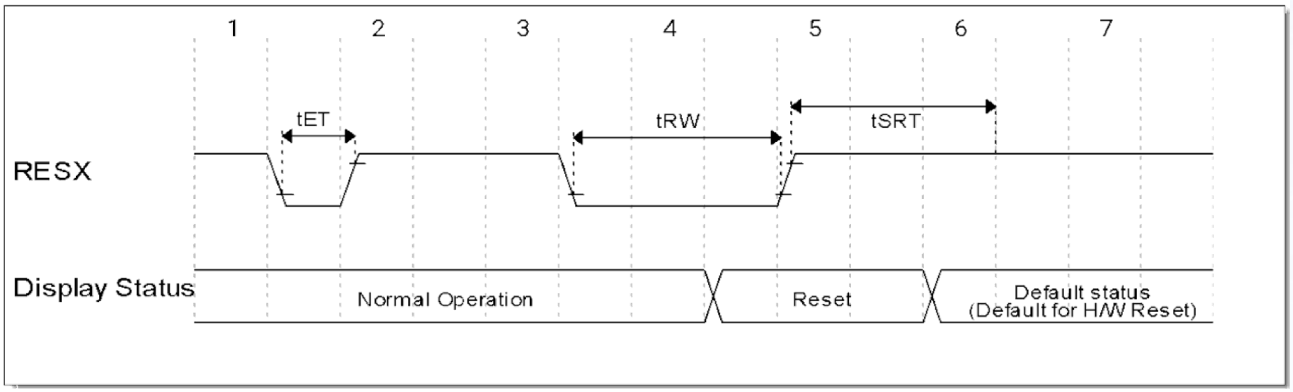


8.2.2 AC Characteristics of MIPI DBI Type-C-Option3 (SPI 4 Wire)

Symbol		Description	Min.	Max.	Unit
CSX	t_{css4}	Chip select setup time	40	-	ns
	t_{csh4}	Chip select hold time	40	-	
	t_{chw4}	Chip select “High" pulse width	50	-	
DCX	t_{as4}	Address setup time	10	-	
	t_{ah4}	Address hold time(Write/Read)	20	-	
SCL (Write)	t_{wc4}	Write cycle time	50	-	
	t_{wrh4}	SCL "High" period (write)	25	-	
	t_{wrl4}	SCL "Low" period (write)	25	-	
SCL (Read)	t_{rc4}	Read cycle time	100	-	
	t_{rdh4}	SCL "High" period (Read)	50	-	
	t_{rdl4}	SCL "Low" period (Read)	50	-	
SDI	t_{ds4}	Data setup time	15	-	
SDI	t_{dh4}	Data hold time	15	-	ns
SDO	t_{acc4}	Access time	5	-	
	t_{od4}	Output disable time	20	-	

Symbol		Description	Min.	Max.	Unit
-	t_r/t_f	Rise/Fall time	-	1	

8.2.3 Timing requirements for RESET



8.2.4 Reset input Timing

Symbol	Description	Min.	Typ.	Max.	Unit
t_{RW}	Reset low pulse width	10	-	-	us
t_{SRT}	Secure reset completion time (Reset during Sleep In mode)	-	-	5	ms
	Secure reset completion time (Reset during Sleep Out mode)	-	-	150	
t_{ET}	Reset un-reacted pulsewidth			5	us

Note:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system according to the table below.

RESX Pulse	Action
Shorter than 5 us	Reset rejected
Longer than 10 us	Reset
Between 5 us and 10 us	Reset start

2. During the reset period, the display will be blanked(The display is entering blanking sequence,for which the maximum time is 150ms,when Reset starts is Sleep Out-mode, The display remains in the blank state in Sleep In-mode) and then return to Default condition for H/W reset.
3. During Reset Completion Time,ID bytes(or similar) value in OTP will be latched to the internal register during this period.This loading is done every time when there is H/W reset complete time(t SRT) within 5ms after a rising edge of RESX.